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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/430,366 | 10/28/1999 | MARK T. RAMSBEY | M-7523-US | 7206 |

24251 7590 02/12/2002

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| EXAMINER |
|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2813 | 16 |

DATE MAILED: 02/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

| Application No. | Applicant(s) |
|---|---|
| 09/430,366 | Ramsbey et al. |
| **Examiner** | **Art Unit** |
| Jack Chen | 2813 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on *Nov 13, 2001* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) *1, 3-7, 9-12, and 14-23* is/are pending in the application.

4a) Of the above, claim(s) *16-20* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 3-7, 9-12, 14, 15, and 21-23* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☒ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 15

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

## DETAILED ACTION

### *Specification*

1. The amendment filed 11/13/2001 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: the phrase "depositing an insulator layer of high temperature oxide ***directly*** on *the substrate and the floating gate*" and "the insulator layer forming *sidewalls around the floating gate*" and "the insulator layer forming *sidewalls of high quality oxide around the floating gate*".

Applicant is required to cancel the new matter in the reply to this Office action.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 3-7, 9-12, 14-15, 21-23 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. See new matter rejection above.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 21 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 21, the term "the layer" lack antecedent basis.

Re claim 22, the term "the layer" lack antecedent basis.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

7. Claims 1, 5, 7, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitchell et al., U.S./4,713,142.

Mitchell et al. discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 32 formed on the substrate, which comprises depositing a floating gate layer

on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 33 (fig. 2a); depositing an insulator layer of oxide 37 (CVD oxide, inherently shows the oxide is the high temperature oxide) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 2c); polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2d); and depositing a dielectric layer 39 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-5, cols. 1-6.

8. Claims 1, 5, 7, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu, U.S./6,033,956.

Wu discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 202 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204; depositing an insulator layer of oxide 210 (CVD oxide, inherently shows the oxide is the high temperature oxide) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (inherently shows the insulator layer forming sidewalls around the floating gate to prevent charge leaking from the floating gate, see fig. 2C), wherein the insulator layer is directly on the floating gate; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2c); and depositing a dielectric layer 214 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu, U.S./6,033,956.

Wu discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 202 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204; depositing an insulator layer of oxide 210 (not limited to any particular type CVD methods [i.e., LPCVD, PECVD, etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results. In addition, the disclosure fails to mention the criticality of the LPCVD process) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2c); and depositing a dielectric layer 214 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.

Wu discloses the claimed invention except LPCVD oxide; the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

11. Claims 3, 4, 6, 9, 10, 12, 14-15, 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu, U.S./6,033,956 or Mitchell et al., U.S./4,713,142 taken with Paterson et al., U.S./4,613,956 in view of Yamagishi et al., U.S./5,808,339 and applicant's admitted prior art.

Wu discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 202 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204; depositing an insulator layer of oxide 210 (not limited to any particular type CVD methods [i.e., LPCVD, PECVD, etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results. In addition, the disclosure fails to mention the criticality of the LPCVD process) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2c); and depositing a dielectric layer 214 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.

Mitchell et al. discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 32 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 33 (fig. 2a); depositing an insulator layer of oxide 37 (not limited to any particular type CVD methods [i.e., LPCVD, PECVD, etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results. In addition, the disclosure fails to mention the criticality of the LPCVD process) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 2c); polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2d); and depositing a dielectric layer 39 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-5, cols. 1-6.

Wu and Mitchell et al disclosed the claimed invention except LPCVD oxide. Paterson et al. discloses a method for forming a semiconductor device, which includes depositing the high temperature/quality oxide on the floating gate by LPCVD in order to provide high uniformity and a highly doped floating gate (col. 3, lines 65-col. 4, lines 6 and col. 4, line 67-col. 5, line 47), see figs. 1-8c, cols. 1-10.

The further difference between the instant claims and the prior arts is: polishing the insulator layer by CMP.

Yamagishi et al. (figs. 9A-10D) discloses a method for forming a semiconductor device having a substrate 11 and a tunnel oxide 51 formed on the substrate, which comprises depositing a floating gate layer 53 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 53; depositing an insulator layer of oxide 54 (by CVD) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing (using CMP or etching back; Art recognized equivalents: using CMP or etching back, because these two methods are art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute one for another) the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 10A); and depositing a dielectric layer 55 (ONO) on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-12B, cols. 1-16.

Furthermore, it is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2.

The thickness of claims 3 and 9 are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as energy, dosage, thickness, width; the rate of etching, temperature and concentration would have been obvious:

"Normally, it is to be expected that a change in energy, etching rate, thickness, dosage, temperature, or combination of any of them would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any thickness range suitable to the method in process of Wu or Mitchell et al. in order to optimize the process.

Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Wu or Mitchell et al. with the teaching of Paterson et al. and Yamagishi et al. and Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device. In addition, the subject matter as a whole would have been obvious to one having

ordinary skill in the art at the time the invention was made to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

12. Claims 1, 3-7, 9-12, 14-15, 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al., U.S./5,808,339 or Chan et al., U.S./6,051,467 taken with Sze et al., "ULSI Technology" and in view of Applicant's admitted prior art.

Yamagishi et al. (figs. 9A-10D) discloses a method for forming a semiconductor device having a substrate 11 and a tunnel oxide 51 formed on the substrate, which comprises depositing a floating gate layer 53 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 53; depositing an insulator layer of oxide 54 (by CVD) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 10A); and depositing a dielectric layer 55 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-12B, cols. 1-16.

Chan et al. further discloses a method for forming a semiconductor device having a substrate 10 and a tunnel oxide 16 formed on the substrate, which comprises depositing a floating gate layer 18 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 18; depositing an insulator layer of oxide 30 (by CVD methods, i.e, APCVD or

PECVD) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 5); and depositing a dielectric layer on the planar surface directly (layer 32 is a optional layer, which is well known in the art) over the exposed top surface of the floating gate and the insulator layer, see figs. 1-11, cols. 1-8.

However, the above references do not explicitly shows forming high temperature oxide by using LPCVD method (Note: during the telephone interview dated on 8/3/2001, applicant admitted that this layer is well known in the art and it is formed by LPCVD process, also see the amendment dated on 8/6/2001, furthermore, applicant stated in the specification, other dielectric may used, i.e., see page 3, lines 26-30. In addition, the disclosure fails to mention the criticality of the LPCVD process).

It is well known in the art to form the dielectric by using any CVD process. For example, Sze et al. teaches forming the dielectric by using LPCVD process, such will provide excellent purity and uniformity, confomal step coverage, large wafer capacity, high throughput, etc. Furthermore, it is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2.

Furthermore, the thickness of claims 3 and 9 are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as energy, dosage, thickness, width; the rate of etching, temperature and concentration would have been obvious:

> "Normally, it is to be expected that a change in energy, etching rate, thickness, dosage, temperature, or combination of any of them would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any thickness range suitable to the method in process of Yamagishi et al. or Chan et al. taken with Sze et al. and in view of Applicant's admitted prior art in order to optimize the process.

Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Yamagishi et al. or Chan et al. with the teaching of Sze et al. and Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device (also see above); in addition, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

***Response to Arguments***

13. Applicant's arguments filed 11/13/2001 have been fully considered but they are not persuasive.

Applicant argues that Mitchell et al. does not show depositing an insulator layer **directly** on *the substrate and the floating gate*. However, this is a new matter issue.

Applicant further argues that Mitchell et al. do not show forming the insulator layer having a thickness greater than the thickness of the floating gate. The Examiner disagrees because fig. 2C, layer 37 clearly shows this feature.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in

a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Sze et al. teaches forming the dielectric by using LPCVD process, such will *provide excellent purity and uniformity, confomal step coverage, large wafer capacity, high throughput*, etc. Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

***Conclusion***

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (703) 308-5838. The examiner can normally be reached on Monday-Friday from 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703)306-2794.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jack Chen

February 6, 2002

Tuan H. Nguyen
Primary Examiner